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EXAMINER	
FLOURNOY, HORACE L	
ART UNIT	**PAPER NUMBER**
2189	

DATE MAILED: 10/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/609,277	SPENCER, ANDREW M.	
	Examiner	Art Unit	
	Horace L. Flournoy	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-19 are presented for examination.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 5, and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "...with said memory array..." There is insufficient antecedent basis for this limitation in the claim. Is this limitation referring to the "nonvolatile memory array" in line 2?

Claim 5 recites the limitation "...on an associated region." Is this a different region than discussed in line 2?

Claim 12 recites the limitation " wherein before said detecting the method further comprises." This limitation does not appear to make sense.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Tsunoda et al. (U.S. PG Pub. no. 2003/0028733, hereafter referred to as Tsunoda) with MPCD offered as extrinsic evidence.

With respect to independent claim 1,

"An integrated memory device that comprises: a nonvolatile memory array;" is disclosed in paragraph [0003] and FIG.1 element 102.

The examiner interprets the limitation "nonvolatile memory array" to mean a plurality of nonvolatile memories or a group of interconnected and/or identical nonvolatile memory devices.

Tsunoda discloses in paragraph [0003], "As the data transfer targets all the nonvolatile memories..." Tsunoda teaches the use of a group of nonvolatile memories (array). Also, inherent to the composition of a flash (nonvolatile) memory (FIG.1) device is that it is composed of a smaller memory array(s) of blocks to hold data.

"...and a nonvolatile buffered memory interface integrated on a substrate with said memory array..." is disclosed in paragraphs [0124], [0056], [0107], FIG. 1 element 101, and FIG. 6 elements 606 and 105.

By definition, a buffer is a region of memory reserved for use as an intermediate repository in which data is temporarily held while waiting to be transferred between two locations or devices (Microsoft Computer Dictionary, 5th Ed., page 76). The examiner interprets the limitation "nonvolatile buffered memory interface" to mean a memory (element 101) which has a nonvolatile region (element 102) which connects to the whole memory. Therefore the examiner interprets elements 102 and 103 of FIG. 1 as "buffers" within the memory apparatus 101.

Tsunoda discloses in paragraph [0107], "The flash-buffer transfer circuit 606 executes data transfer between the flash memory 102 and the data buffer 108."

Tsunoda discloses in paragraph [0056], "The memory apparatus 4000 constructs, for example the SDRAM 4010, the flash memory 4020, and the control unit 4030 on different silicon chips, and interconnects terminals of the silicon chips by, for example wire bonding, thereby providing a multichip package, in which the components are sealed in one package. Here, the package indicates an LSI package form such as a thin small outline package (TSOP), or a ball grid array (BGA)." Tsunoda further discloses in paragraph [0124], " The memory apparatus 101, 901, 1301 and 1401 of the present invention can be applied to any shapes. For example, the apparatus may be a

LSI, in which memory chips and a control chip are sealed in one package, or all the functions may be housed on one semiconductor chip."

Tsunoda teaches a nonvolatile buffered memory interface (flash-buffer transfer circuit 606) integrated on a substrate (all the functions may be housed on one semiconductor chip) with said memory array(FIGs. 1 and 6). FIG. 1 shows the memory apparatus which integrates the nonvolatile buffered memory interface (element 105) and the memory array (element 102).

"...wherein the memory interface comprises:

one or more volatile buffers configured to buffer data for read operations..." is disclosed in paragraph [0110].

The examiner interprets this limitation as a volatile buffer that is used for read operations or as data.

Tsunoda discloses in column [0110], "The read sector data (SCTn) is transferred...from the data buffer 108 through the SDRAM-buffer transfer circuit 607 and the MUX/DEMUX 0 (609) to the SDRAM interface control circuit 107, and written in the SDRAM 103." Tsunoda teaches a volatile buffer(SDRAM-buffer) configured to buffer data (transfer) for read operations (read data).

"...a table memory configured to indicate one or more addresses associated with data buffered in the one or more volatile buffers" is disclosed in paragraphs [0105] and [0107].

Tsunoda discloses in paragraph [0105], "FIG. 6 shows an internal configuration of the data transfer control unit 105. The data transfer control unit 105 includes a command decoder 601, a sequencer 602, an address mapping table 603, a flash address (ADRf1) generation circuit 604, a sector counter 605, a flash-buffer transfer circuit 606, an SDRAM-buffer transfer circuit 607, an SDRAM address (ADRsd) generation circuit 608, an MUX/DUXEMUX 0 (609), a buffer address (ADRbu) generation circuit 610, and an MUX/DEMUX 1 (611)." Tsunoda teaches a memory or table (address mapping table 603) that is configured to one or more addresses associated with data buffered in the one or more volatile buffers (SDRAM-buffer).

With respect to claim 2,

> "The device of claim 1 , wherein the table memory is volatile, and wherein the memory interface is configured to preserve contents of the table memory in nonvolatile memory during absences of electrical power" is disclosed in paragraph [0112].

The examiner interprets claim 2 to mean a volatile memory that uses a memory interface that is configured to preserve the contents of the volatile memory in nonvolatile memory during absences of electrical power.

Tsunoda discloses in paragraph [0112], "by transferring the data on the SDRAM 103 to the flash memory 102, the data can be held even after the power is turned off."

With respect to claim 3,

"The device of claim 2, wherein the memory interface is further configured to restore the contents of table memory from the nonvolatile memory when electrical power returns" is disclosed in paragraphs [0098] and [0099].

The examiner interprets claim 3 as the memory interface being further configured to restore the contents of table or volatile memory from the nonvolatile memory when electrical power returns.

Tsunoda discloses in paragraphs [0098] and [0099], "Since the SDRAM 103 is a volatile memory, the information stored in the nonvolatile area 204 on the SDRAM 103 is copied to the flash memory 102 before the power is turned OFF, and held on the flash memory 102... [0099] Use of the foregoing address space on the SDRAM 103 enables the following processing to be executed. After the power is turned ON, program data on the flash memory 102 is copied to the volatile area 203 of the SDRAM 102, and the host 111 can use the program by accessing the volatile area 203 on the SDRAM 103.

With respect to claim 4,

"The device of claim 1, wherein when electrical power returns, the memory interface is further configured to restore the one or more volatile buffers to a state preceding the absence of electrical power" is disclosed in paragraphs [0098] and [0099].

The examiner interprets claim 4 to mean when electrical power returns, the memory interface is further configured to restore the one or more volatile buffers to a state preceding the absence of electrical power.

Tsunoda discloses in paragraphs [0098] and [0099], "Since the SDRAM 103 is a volatile memory, the information stored in the nonvolatile area 204 on the SDRAM 103 is copied to the flash memory 102 before the power is turned OFF, and held on the flash memory 102... [0099] Use of the foregoing address space on the SDRAM 103 enables the following processing to be executed. After the power is turned ON, program data on the flash memory 102 is copied to the volatile area 203 of the SDRAM 102, and the host 111 can use the program by accessing the volatile area 203 on the SDRAM 103."

Tsunoda teaches when electrical power returns (power turned ON), the memory interface is further configured to restore the one or more volatile buffers (SDRAM 102) to a state preceding the absence of electrical power (program data which was copied to the nonvolatile memory).

With respect to claims 5 and 18,

"The device of claim 1, wherein the one or more volatile buffers comprise:

a plurality of read buffers each associated with a different region of the memory array and configured to buffer only data for read operations on an associated region"

and

"The device of claim 15, wherein the one or more read buffers comprise: a plurality of read buffers each associated with a different region of the memory and configured to buffer only data for read operations on an associated region" are disclosed in paragraph [0107] and FIG. 6.

The examiner interprets claims 5 and 18 to mean the read buffers (or volatile buffers) comprise: a plurality of read buffers each associated with a different region of the memory and configured to buffer only data for read operations on an associated region.

Tsunoda discloses in paragraph [0107], "The mapping table 603 is for allocating the nonvolatile area 204 on the address space in the SDRAM 103 to the logical sector address 205 of the flash memory 102. The ADRf1 generation circuit 604 generates a logical sector address on the flash memory 102. ... In reading, data of the SDRAM 103 sent from the SDRAM interface control circuit 107 is sent to the data bus of the SDRAM interface 112 connected to the host, or the SDRAM-buffer transfer circuit 607."

Tsunoda teaches the read buffers (or volatile buffers) comprise: a plurality of read buffers (address space in the SDRAM) each associated(allocated the nonvolatile area) with a different region (logical sector) of the memory (flash memory) and configured to buffer only data for read operations on an associated region.

With respect to claim 6,

"The device of claim 1, wherein the memory array comprises magnetic random access memory (MRAM) cells" is disclosed in paragraph [0124].

Tsunoda discloses in paragraph [0124], "Further, types of the nonvolatile memory and the volatile memory of the present invention are not limited to the flash memory 102 or the SDRAM 103. For example, regarding the nonvolatile memory, similar processing can be carried out in a ferroelectric memory or an MRAM (magnetic memory)."

With respect to claims 7 and 19,

"The device of claim 1, wherein the memory interface further comprises;

an interface control module that is configured to receive read commands specifying a memory address..." is disclosed in paragraph [0105], [0109], and FIG. 6.

The examiner interprets this claim to mean the memory interface further comprises an interface control module that is configured to receive read commands specifying a memory address.

Tsunoda discloses in paragraph [0105], "FIG. 6 shows an internal configuration of the data transfer control unit 105. The data transfer control unit 105 includes a command decoder 601, a sequencer 602, an address mapping table 603, a flash address (ADRf1) generation circuit 604, a sector counter 605, a flash-buffer transfer circuit 606, an SDRAM-buffer transfer circuit 607, an SDRAM address (ADRsd)

generation circuit 608, an MUX/DUXEMUX 0 (609), a buffer address (ADRbu) generation circuit 610, and an MUX/DEMUX 1 (611). The command decoder 601 interprets a content of the command issued by the host 111. The sequencer 602 manages entire processing of the data transfer control unit 105." Tsunoda further discloses in paragraph [0109], "the host 111 issues a command (address 6 in FIG. 3) for setting a transfer start address Ctx 212 of the SDRAM 103. The Ctx 212 is held in the ADRsd generation circuit 608."

Tsunoda teaches a memory interface (stated supra) which further comprises an interface control module (data control unit, element 105 of FIG.6) that is configured to receive (element 608 of FIG. 6) read commands specifying a memory address (the host 111 issues a command (address 6 in FIG. 3) for setting a transfer start address Ctx 212 of the SDRAM 103).

"...wherein the interface control module is coupled to the memory array..." is disclosed in FIG. 1 elements 102,103, and 105.

Tsunoda discloses in FIG. 1 the interface control module (data transfer control unit, element 105) is coupled to the memory array(elements 102 and 103).

"...to conduct read operations to satisfy the read commands and to prepare read buffers to satisfy anticipated read commands" is disclosed in paragraph [0107].

The examiner interprets this claim to mean the memory array comprises magnetic random access memory (MRAM) cells.

Tsunoda discloses in paragraph [0107], "In reading, data of the SDRAM 103 sent from the SDRAM interface control circuit 107 is sent to the data bus of the SDRAM interface 112 connected to the host, or the SDRAM-buffer transfer circuit 607...When data is read from the data buffer 108, the data is sent to the flash-buffer transfer circuit 606 or the SDRAM-buffer transfer circuit 607."

Tsunoda teaches conducting read operations (reading) to satisfy the read commands (from host, discussed supra) and to prepare read buffers to satisfy anticipated read commands (data is sent to the flash-buffer transfer circuit 606 or the SDRAM-buffer transfer circuit 607).

With respect to claims 8 and 19,

"The device of claim 7, further comprising: an error correction code (ECC) decoder coupled between the memory array and the one or more volatile buffers" is disclosed in paragraph [0097] and FIG. 1 element 109.

Tsunoda discloses in paragraph [0097], "an ECC control circuit 109 in the flash memory interface control unit 106 checks whether an errors is present or not in data read from the flash memory 102, and corrects the data if an error is present."

Tsunoda teaches in FIG. 1 an error correction code (ECC) decoder (element 109) coupled between the memory array (element 102) and the one or more volatile buffers (element 105 and element 607 of FIG.6).

With respect to independent claim 9,

"A method of providing access to stored data, the method comprising: preserving during an absence of electrical power information indicative of data in one or more read buffers; and restoring the data to the one or more read buffers when power returns" is disclosed in paragraphs [0098] and [0099].

The examiner interprets claim 9 to mean a method for providing access to stored data which includes preserving during an absence of electrical power (power is turned OFF) information indicative of data in one or more read buffers; and restoring the data to the one or more read buffers when power returns.

Tsunoda discloses in paragraphs [0098] and [0099], "Since the SDRAM 103 is a volatile memory, the information stored in the nonvolatile area 204 on the SDRAM 103 is copied to the flash memory 102 before the power is turned OFF, and held on the flash memory 102... [0099] Use of the foregoing address space on the SDRAM 103 enables the following processing to be executed. After the power is turned ON, program data on the flash memory 102 is copied to the volatile area 203 of the SDRAM 102, and the host 111 can use the program by accessing the volatile area 203 on the SDRAM 103."

Tsunoda teaches a method for providing access to stored data which includes preserving during an absence of electrical power (power is turned OFF) information indicative of data (program data) in one or more read buffers (SDRAM); and restoring the data to the one or more read buffers (program data on the flash memory 102 is

copied to the volatile area 203 of the SDRAM 102) when power returns(power is turned ON).

With respect to claims 10 and 17,

"The device of claim 9, wherein said preserving comprises:

detecting a pending power-down;

for each of the one or more read buffers, storing in nonvolatile memory a starting address associated with data in the read buffer" is disclosed in paragraphs [0046], [0047], [0100], and FIG. 5.

The examiner interprets claim 10 to mean detecting a pending power-down and storing in nonvolatile memory a starting address associated with data in the read buffer.

Tsunoda discloses in paragraphs [0046] and [0047], "By the storage function, the data transferred to the flash memory 4020 can be held on the flash memory 4020 even if it is lost from the SDRAM 4010 because of a stop of the power supply to the memory apparatus 4000...The storage function is executed when an operation status of the memory apparatus 4000 satisfies predetermined storage execution conditions. One of the storage execution conditions is, for example a stop of the power supply."

Tsunoda also discloses in paragraph [0100], "...a head address (ADRsdA 209) of the command/status holding area 202 to be accessed first by the host is stored beforehand in the register or the flash memory 102 in the memory apparatus 101. An address 4 designates a format of the flash memory 102, an address 5 a start sector

address (Dtx 213) in data transfer to the flash memory 102 or erasure, an address 6 data transfer start address (Ctx 212) to the SDRAM 103..."

Tsunoda teaches detecting a pending power down (predetermined storage execution condition...a stop of the power supply). Tsunoda further teaches storing in nonvolatile memory (flash memory) a starting address (data transfer start address (Ctx 212)) associated with data in the read buffer for each of the read buffers (SDRAM).

With respect to claims 11 and 14,

"The method of claim 10, wherein said restoring comprises for each of the one or more read buffers:

accessing the nonvolatile memory to retrieve the starting address associated with the read buffer; and

filling the read buffer with data from a memory array, beginning with data associated with the starting address" is disclosed in paragraph [0100] and FIG. 5.

The examiner interprets claim 11 to mean accessing the nonvolatile memory to retrieve the starting address associated with the read buffer, and filling the read buffer with data from a memory array, beginning with data associated with the starting address.

Tsunoda also discloses in paragraph [0100], "...a head address (ADRsdA 209) of the command/status holding area 202 to be accessed first by the host is stored beforehand in the register or the flash memory 102 in the memory apparatus 101. An

address 4 designates a format of the flash memory 102, an address 5 a start sector address (Dtx 213) in data transfer to the flash memory 102 or erasure, an address 6 data transfer start address (Ctx 212) to the SDRAM 103, an address 7 a data transfer size between the flash memory 102 and the SDRAM 103, or a data erasure size of the flash memory 102, an address 8 a start of data transfer between the flash memory 102 and the SDRAM 103, and an address 9 a power saving mode."

Tsunoda teaches accessing the nonvolatile memory to retrieve the starting address associated with the read buffer (a head address (ADRsdA 209) of the command/status holding area 202 to be accessed first by the host is stored beforehand in the register or the flash memory 102 in the memory apparatus 101). FIG. 5 teaches filling the read buffer with data from a memory array, beginning with data associated with the starting address. In regard to claim 14, the limitation "wherein the one or more read buffers are integrated on a substrate with a nonvolatile memory array..." is stated supra.

With respect to claim 12,

> "The method of claim 10, wherein before said detecting the method further comprises: receiving a read command that comprises a read address..." is disclosed in paragraph [0052].

The examiner interprets the limitation to mean the method of detecting includes a read command that comprises a read address.

Tsunoda discloses in paragraph [0052], "The memory apparatus 4000 includes a function for enabling the host 4040 to designate changing of the address correspondence setting information. The memory apparatus 4000 includes a function of saving the address correspondence setting information in the flash memory 4020. The memory apparatus 4000 includes a function of reading the address correspondence setting information from the flash memory 4020."

Tsunoda teaches a read command that comprises a read address (host to designate changing of the address correspondence setting information).

"...determining whether data from the read address is buffered in a read buffer..." is disclosed in paragraphs [0050] and [0051].

The examiner interprets this limitation to mean determining whether data from the read address is buffered in a read buffer.

Tsunoda discloses in paragraphs [0050] and [0051], "The memory apparatus 4000 includes a function of reading the load execution condition information from the load execution condition information. The memory apparatus 4000 includes a function of setting a correspondence between an address of the SDRAM 4010 and an address of the flash memory 4020 according to a predetermined process. [0051] Data transfer in the storage function and the load function is carried out between addresses made corresponding to each other by the address correspondence setting function. The address correspondence setting function is executed based on address correspondence setting information."

"...retrieving data from a location in a memory array associated with the read address if the data is not buffered..." is disclosed supra in claim 9.

"...and responding to the read command with data from said one of the plurality of read buffers if the data is buffered" is disclosed supra in claim 7.

With respect to independent claim 13,

"A method of providing access to stored data, the method comprising: preserving during an absence of electrical power information indicative of data in one or more read buffers; when power returns, determining whether a restore operation is enabled', and if the restore operation is enabled, restoring the data to the one or more read buffers when power returns." is disclosed in paragraphs [0073]-[0078], [0098] and [0099].

The limitations "A method of providing access to stored data, the method comprising: preserving during an absence of electrical power information indicative of data in one or more read buffers... and if the restore operation is enabled, restoring the data to the one or more read buffers when power returns" are stated supra in claim 9. The examiner interprets the limitation "...when power returns, determining whether a restore operation is enabled..." to mean indicating whether a restore or load back operation is enabled or signaled.

Tsunoda discloses in paragraph [0078], "A power supply start 4061 is a path, in which data is loaded from the mirror area 4021 to the nonvolatile area 4010 when the power supply to the memory apparatus 4000 is started. Load 4062 is a path, in which data is loaded from the mirror area 4021 to the nonvolatile area 4010, for example when the host 4040 issues a load execution instruction to the memory apparatus 4000."

Tsunoda teaches when power returns (power ON or power supply to the memory apparatus 4000 is started) , determining whether a restore operation is enabled (the host 4040 issues a load execution instruction to the memory apparatus 4000).

With respect to claim 15,

"A digital device that comprises:

a memory having a nonvolatile buffered memory interface with one or more read buffers..." is disclosed as stated supra.

"...and a processor coupled to the memory device and configured to retrieve stored information from the memory..." is disclosed in paragraphs [0004], [0005], [0040] and FIG. 1 elements 111 and 1112.

The examiner interprets this limitation to mean a processor is coupled (connected) to the memory device and configured to retrieve stored information from the memory.

Tsunoda discloses in paragraphs [0004] and [0005], "An object of the present invention is to provide a memory apparatus, which enables a host to control data transfer between a volatile memory and a nonvolatile memory, and controllability from the host to be improved...Another object of the present invention is to provide a memory apparatus, which enables a host to access a nonvolatile memory, and controllability from the host to be improved." Tsunoda further discloses in paragraph [0040], "...the host 4040 is an information processor such as a CPU or ASIC incorporated in the information terminal. In the memory apparatus 4000, operation programs for, for example, enabling the host 4040 to execute various information processing, can be stored."

Tsunoda teaches a processor (host: element 111) is coupled to (element 112) the memory device (memory apparatus: element 101) and configured to retrieve stored information from the memory(host to access a nonvolatile memory).

> "...wherein the processor causes the memory to receive a power down command before electrical power is removed from the memory, and wherein the memory interface responsively stores in a nonvolatile memory information indicative of data in said one or more read buffers." is disclosed in paragraphs [0046] and [0047].

The examiner interprets this limitation to mean, the processor causes the memory to receive a power down command before electrical power is removed from the memory, and wherein the memory interface responsively stores in a nonvolatile

memory information indicative of data in one or more read buffers.

Tsunoda discloses in paragraphs [0046] and [0047], "...the host 4040 can issue a reading command, a writing command, a refreshing command or the like to the memory apparatus 4000. The memory apparatus 4000 includes a storage function of transferring data held in a predetermined area of the SDRAM 4010 to a predetermined area of the flash memory 4020. By the storage function, the data transferred to the flash memory 4020 can be held on the flash memory 4020 even if it is lost from the SDRAM 4010 because of a stop of the power supply to the memory apparatus 4000....The storage function is executed when an operation status of the memory apparatus 4000 satisfies predetermined storage execution conditions. One of the storage execution conditions is, for example a stop of the power supply."

Tsunoda teaches the processor causes the memory to receive a power down command (command to memory apparatus 4000...storage execution condition) before electrical power is removed from the memory, and wherein the memory interface responsively stores in a nonvolatile (flash) memory information indicative of data in one or more read buffers(SDRAM).

With respect to claim 16,

"The device of claim 15, wherein the memory interface is further configured to reload the one or more read buffers with data in accordance with information

from the nonvolatile memory when power returns" is disclosed in paragraphs [0098] and [0099] and FIGs. 1, 2, and 24.

The examiner interprets claim 9 to mean the memory interface is further configured to reload (restore) the one or more read buffers (SDRAM) with data in accordance with information from the nonvolatile memory when power returns.

Tsunoda discloses in paragraphs [0098] and [0099], "Since the SDRAM 103 is a volatile memory, the information stored in the nonvolatile area 204 on the SDRAM 103 is copied to the flash memory 102 before the power is turned OFF, and held on the flash memory 102... [0099] Use of the foregoing address space on the SDRAM 103 enables the following processing to be executed. After the power is turned ON, program data on the flash memory 102 is copied to the volatile area 203 of the SDRAM 102, and the host 111 can use the program by accessing the volatile area 203 on the SDRAM 103."

Tsunoda teaches the memory interface is further configured to reload (copy) the one or more read buffers (volatile area 203 of FIG. 2 of the SDRAM) with data in accordance with information (program data) from the nonvolatile memory (flash memory) when power returns (after the power is turned ON).

Conclusion

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Horace L. Flournoy whose telephone number is (571) 272-2705. The examiner can normally be reached on Monday-Friday 7:00 AM to 4:30 PM (ET).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Don Sparks can be reached on (571) 272-4201. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 746-7239

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

CHRISTIAN CHACE
PRIMARY EXAMINER

Horace L. Flournoy

Patent Examiner

Art unit: 2189

Primary Patent Examiner

Technology Center 2100